I claim

1. A conversion circuit for converting burst signal referencing to a plurality of clocks including at least a first clock and a second clock, the conversion circuit comprising

a plurality of phase signal generators, each of the phase signal generators receiving signals of said first clock at an input end thereof and generating a phase signal;

a plurality of signal fetching units with number corresponding to that of said phase signal generators, each of said signal fetching units having one input for receiving a burst signal referencing to said first clock and another input connected to said corresponding phase signal generator for receiving a phase signal;

a plurality of converters with number corresponding to that of said signal fetching units, each of said converters having one input for receiving signals of said second clock and another input for receiving an output signal of said corresponding signal fetching unit; and

a signal synthesizer having a plurality of input ends connected to respective output of said corresponding converter for combining the output signals from said converters into a signal referencing to said second clock.

2. The conversion circuit as recited in claim 1, wherein each of said phase signal generators generates phase signals with one cycle of high-voltage logic state and at least one cycle of low-voltage logic state in cyclic manner.

3. The conversion circuit as recited in claim 2, wherein only one phase signal from those phase signal generators is in high-voltage logic state during one cycle of said first clock.

4. The conversion circuit as recited in claim 2, wherein each of said signal fetching units fetches said burst signal referencing to said first clock when corresponding phase signal generator generates a signal in high-voltage logic state.

5. The conversion circuit as recited in claim 2, wherein each of said signal fetching units is an AND gate.

6. The conversion circuit as recited in claim 1, wherein each of said converters is a latch.

7. The conversion circuit as recited in claim 6, wherein each of said latchs samples said output signal of said corresponding signal fetching unit with reference to said second clock.

8. The conversion circuit as recited in claim 1, wherein said signal synthesizer is an OR gate.

9. The conversion circuit as recited in claim 1, wherein said second clock has a frequency higher than that of said first clock.

10. A method for converting burst signal referencing to at least two clocks, said method comprising the steps of:

providing a first clock and a second clock;

providing a burst signal referencing to said first clock;

decomposing said burst signal into a plurality of non-burst signals;

converting said plurality of non-burst signals into signals referencing to said second clock; and

synthesizing said non-burst signals referencing to said second clock into an output signal.

11. The method as recited in claim 10, wherein the step of decomposing said burst signal into a plurality of non-burst signals comprises following sub-steps:

providing a plurality of phase signal generators and a plurality of signal fetching units with number corresponding to that of said phase signal generators;

generating a plurality of phase signals from said plurality of phase signal generators and sending said plurality of phase signals to corresponding signal fetching units;

fetching said burst signal referencing to said first clock by said signal fetching units with reference to corresponding phase signal.

12. The method as recited in claim 11, wherein each of said phase signal generators generates phase signals with one cycle of high-voltage logic state and at least one cycle of low-voltage logic state in cyclic manner.

13. The method as recited in claim 12, wherein only one phase signal from said phase signal generators is in high-voltage logic state during one cycle of said first clock.

14. The method as recited in claim 12, wherein each of said signal fetching units is an AND gate.

15. The method as recited in claim 10, wherein each of said converters is a latch.

16. The method as recited in claim 15, wherein each of said latchs samples corresponding non-burst signals with reference to said second clock.

17. The method as recited in claim 16, wherein each of said latchs samples corresponding non-burst signal at rising edge of said second clock.

18. The method as recited in claim 17, wherein each of said latchs does not sample corresponding non-burst signal at next cycle of second clock once said non-burst signal is latched.

19. The method as recited in claim 10, wherein the step of synthesizing said signals referencing to said second clock into an output signal comprises following sub-steps:

providing a signal synthesizer; and

synthesizing said signals referencing to said second clock into said output burst signal by said signal synthesizer.

20. The method as recited in claim 19, wherein said synthesizer is an OR gate.

21. The method as recited in claim 10, wherein said second clock has a frequency higher than that of said first clock.